AN 8–BIT PROGRAMMABLE FINE DELAY CIRCUIT WITH STEP SIZE 65PS FOR AN ULTRAWIDEBAND PULSE POSITION MODULATION TESTBED

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ABSTRACT

This contribution discusses the design of a programmable delay shifter for an ultrawideband (UWB) pulse position modulation (PPM) testbed. PPM was selected because of its low duty cycle which translates to high power efficiency. The receiver synchronisation subsystem uses a digitally controlled delay shifter which is implemented in two parts: a coarse and a fine shifter. The resulting delay shift circuit is controlled by an 8-bit word and is designed to realise the delays with a granularity of 65.1 ps. The proposed combination of the delay step and fine delay components is a viable solution and the power consumption is comparable to a DDS solution.

1. INTRODUCTION

The pioneering UWB industry has demonstrated that the basic physical layer technology works, but many system-level and operational issues remain that need to be investigated before UWB technology can be integrated into commercial devices [1].

Currently, there exists just a very small number of methods for generating signals having ultrawide bandwidth: e.g. chirp modulation, direct spreading by high-rate pseudo-random noise sequences [2, 3], fast frequency hopping [4, 5], and transmission via short pulses [6, 7, 8, 9]. The latter option was chosen because of its simplicity in circuitry and its inherently low power consumption. Among the possible modulation formats, PPM was favored because it allows incoherenct detection which eases receiver design and relaxes synchronisation requirements.

The testbed is implemented using off-the-shelf electronic components only. The testbed consists of a transmitter and a receiver part. The data transmission is unidirectional and realizes data transmission at 6 Msymb/s over a distance of a few meters in indoor office environments. The ultimate goal is to develop commercial-grade microwave circuitry and algorithms for ultra-wideband data transmission, especially concerning small battery driven devices. An overview over the testbed is given and the delay shifter is discussed in detail. The two-stage approach used for UWB PPM receiver synchronisation can be summarised as (i) initial symbol rate acquisition (ii) subsequent continuous delay tracking. The signal processing algorithms are published and discussed in [10].

The receiver estimates the pulse repetition frequency once and sets the local voltage-controlled crystal oscillator (VCXO) to this estimate. Subsequently, an early-late tracker controls an eight-bit programmable delay shifter with a granularity of 65.1 ps and the local VCXO. The whole synchronisation algorithm is implemented on a low-cost microcontroller (μC).

Measurement results obtained from the testbed are discussed and compared to simulations in Matlab.

2. RECEIVER

The receiver architecture is shown in Figs. 1 and 2. Low-noise amplifiers (LNA) are used in the front-end for increasing the signal amplitude and to ensure a sufficient signal-to-noise ratio for the down conversion. The LNAs consist of InGaP/GaAs MMIC (NBB-300, RF Micro Devices Inc.). A Wilkinsom power divider splits the received signal into five branches of same strength. Five sampling mixers sample the input signal at different delays provided by a tapped delay line. Each of the five branches has one sampling mixer. The fifth branch of the receiver aids the synchronisation.

The tapped delay line is implemented in the integrated circuit 3D3215 (Data Delay Devices Inc.). This component implements five nominally equally spaced taps of $T = 2\,\text{ns}$ delay each. Some delay tolerances have been observed which are also due to differences in the capacitive loads. These load differences have been compensated by introducing small parallel capacitors.

Another set of five lowpass filters is used for the synchronisation part of the receiver (see Fig. 2). It averages the energy of a high number of symbols and suppresses interference. A five-channel analog-to-digital converter (ADC) samples all inputs simultaneously. A μC is used for executing the synchronisation algorithm and fulfills several other tasks in the testbed. A clock generator delivers the timebase of the receiver: it is frequency controlled by the μC.

The received PPM signal $r(t)$ at the frontend of the receiver can be modelled as

$$r(t) = \sum_{k=-\infty}^{\infty} q(t - A_{\lfloor k/10 \rfloor} T - kT_{\text{PRF}} - \tau(t)) + n(t)\,, \qquad (1)$$

where $q(t)$ denotes the overall pulse shape, $T = 2\,\text{ns}$ is the timeslot duration, $f_{\text{PRF}} = \frac{1}{T_{\text{PRF}}} = 60\,\text{MHz}$ is the PRF, and $n(t)$ denotes the noise. The pulse shape $q(t)$ results from the linear distortions between the antenna connectors at the transmitter and the receiver.

The sampling mixers are clocked synchronously at the receiver's estimate of the PRF which is denoted by $\hat{f}_{\text{PRF}} = (\hat{T}_{\text{PRF}})^{-1}$.

The ℓth sampling mixer ($\ell = 0, 1, \ldots, 4$) is triggered at the delay $\ell T + \varepsilon_\ell + \hat{\Delta}(t)$ where $\hat{\Delta}(t)$ is adjusted by the μC

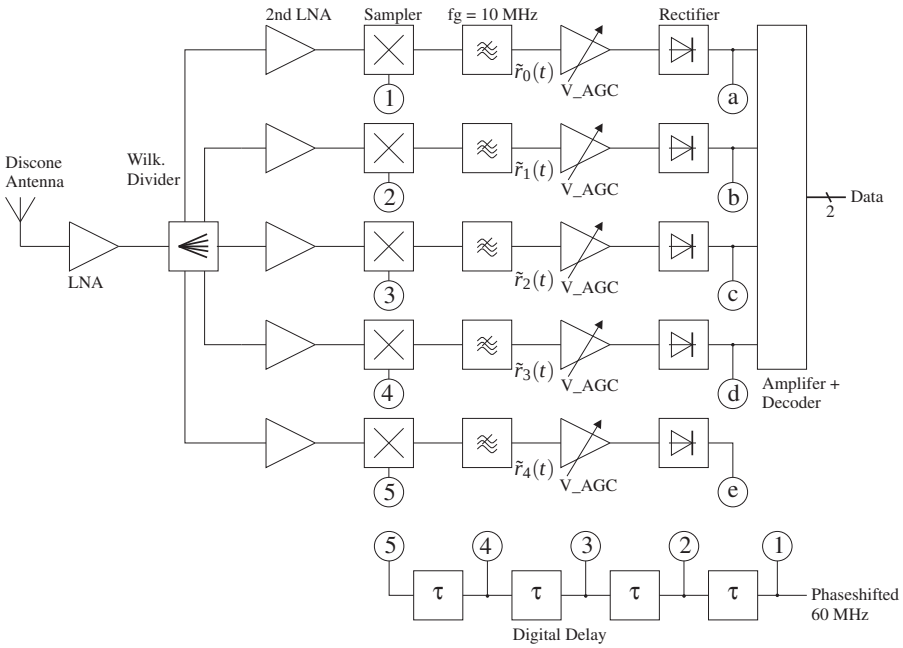

Figure 1: Block diagram of the data path of the receiver.

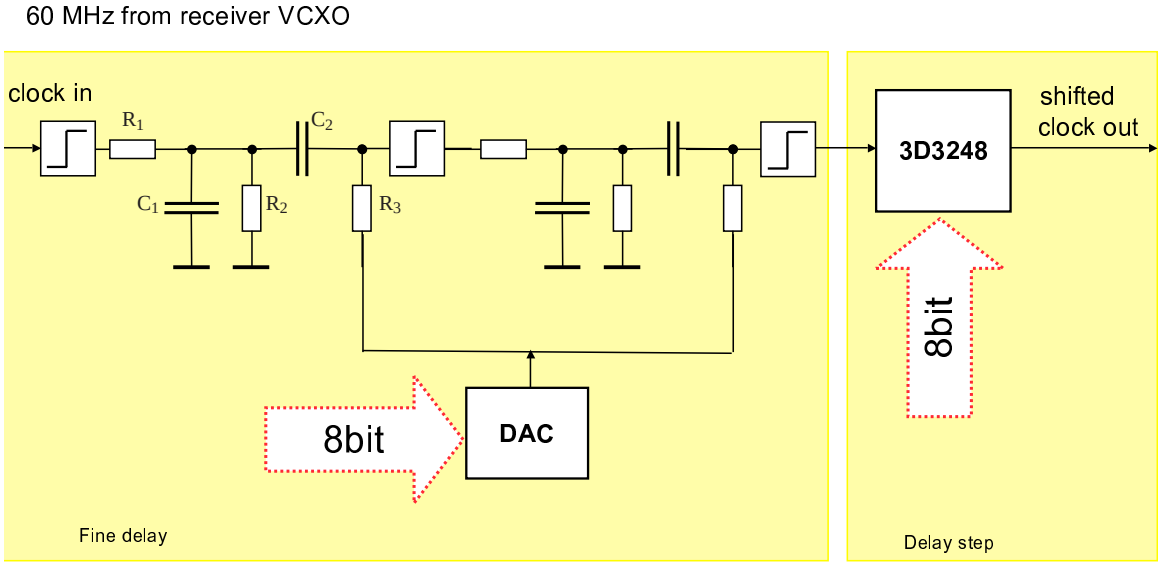

Figure 3: Schematic of the "Finedelay" and "Delay step".

using the *Delay Step* and *Finedelay* (see p. 3), and $|\varepsilon_\ell| \ll T$ describes small constant delay deviations from the PPM symbol delay slots at ℓT, i.e. we designed an early-late sampler with $\varepsilon_0 \approx \varepsilon_3 \approx -100\,\text{ps}$ and $\varepsilon_1 \approx \varepsilon_2 \approx 100\,\text{ps}$.

After the sampling mixer in the ℓth signal path of the receiver, we obtain for $\ell = 0, 1, \ldots, 4$

$$\tilde{r}_\ell(t) = \sum_{n=-\infty}^{\infty} r(t)\ \delta(t - n\hat{T}_{\text{PRF}} - \ell T - \varepsilon_\ell - \hat{\Delta}(t))\ . \quad (2)$$

2.1 Local Oscillator Pulse Generation

The only difference of the five receiver paths is the position of the local oscillator pulses which control the diodes in the

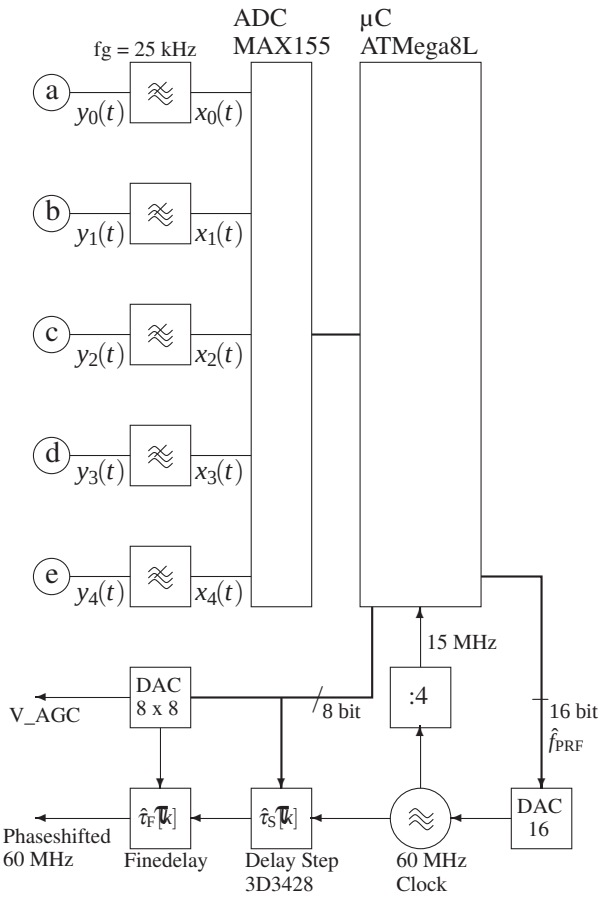

Figure 2: Synchronisation and control components of the receiver. The inputs a, b, . . . , e are connected to the corresponding points in Fig. 1.

sampler circuit.

The main receiver clock of 60 MHz is the source for generation of the local oscillator pulses. The same digital delay line like the one used in the transmitter is also applied in the receiver. The distance is adjusted to equidistance plus or minus a small fraction. So two early and two late LO signals are generated. This is used to detect the exact position in the time frame of the incoming signal.

A CPLD generates the rising edges used in the pulse sharpening circuit. In a later stage, it is foreseen to implement a time hopping sequence generator in the CPLD for mitigating multiple access interference.

Just a single transistor stage is necessary in the pulse shaper of the receiver because the amplitude and impedance requirements are not stringent.

It is controlled by the μC by means of an 8 Bit DAC channel.

Digital to Analog Converter (DAC).

An eight-channel DAC is integrated into the receiver circuitry for three different tasks. The first task is to set the gain of the variable gain amplifier. In this way, the automatic gain control (AGC) loop is closed. The second task is to control the Finedelay circuitry shown in Fig. 2. In this way, the receiver's clock timing can be delayed in steps of $T_{\mathrm{PRF}}/256$.

3. DIGITALLY CONTROLLED DELAY SHIFTER.

The receiver synchronisation subsystem uses a digitally controlled delay shifter, comprising the *Delay Step* and *Finedelay* blocks in Fig. 1. The delay shifter is controlled by a pair of 8-bit words which are stored in a lookup table.

The delay shifter is controlled by an 8-bit word $d \in \{0, 1, \ldots, 255\}$ and is designed to realise the delay $d\Delta$ with a granularity of $\Delta = 65.1\,\mathrm{ps}$. This results in delays up to $\frac{255}{256} T_{\mathrm{PRF}} \approx 16.60\,\mathrm{ns}$.

The schematic of the implementation is shown in Fig. 3. The controlled delay shifter is implemented in two stages, *Delay Step* and *Finedelay*, respectively. The *Delay Step* is based on an 8-bit controllable delay circuit (3D3428-0.25 from Data Delay Devices Inc.) having nominal delay steps of 0.25 ns. This granularity is too coarse for timing adjustment of the receiver. Therefore, a second stage, *Finedelay*, is serially concatenated with a range of delay shifts of approx. 1 ns. The *Finedelay* is controlled by one analog output voltage of the 8-bit DAC. The observed average delay behaviour of 3D3428-0.25 is shown in Fig. 5(a). The delay steps are non-uniform and evidently too coarse for synchronising to a pulse width smaller than 100 ps.

The Finedelay circuit is shown in the left part of Fig. 3. The clock input is transformed into a periodic sawtooth signal by the first RC lowpass filter (R_1, C_1, R_2) and then C_2 removes the DC offset of the first gate. Next, the D/A output is added to the sawtooth via R_3 before entering a second stage with the same functionality. The observed average delay (ns) behaviour of the Finedelay circuit is shown in Fig. 5(b). We observe the generally non-linear input-output relation and that this behaviour is not monotonous. These errors in monotonicity are deterministic which was confirmed by repeated delay measurements. They are due to monotonicity errors in the off-the-shelf D/A converter.

We define the implementation error of the realised device as the difference between the implemented delay and the desired delay $d\Delta$. Finally, we carried out a discrete optimization over pairs of 8-bit words for each desired delay shift $\tau = d\Delta$ for $0 \le d \le 255$ such that the absolute delay shift implementation error is minimum for each d. The optimum pair of words was stored in a lookup table.

In this way, we implemented a digitally controlled delay adjustment in 256 quantised steps with a stepsize of approx. 65.1 ps. The implementation error (in pico seconds) of the realised delay is shown in Fig. 5 versus the digital input value.

4. CONCLUSION

In Impulse Radio UWB systems, fine-granularity delay shifters and low-jitter oscillators are required. Suitable components are not available off-the-shelf. Therefore, we needed to implement a digitally controlled delay shifter with almost uniform stepsize $\approx 65.1\,\mathrm{ps}$ in the testbed. The combination of the delay step and fine delay components is a viable solution and the power consumption is comparable to a DDS solution. The jitter of the proposed solution is better than a DDS with 10 bit D/A converter. The latency for changes in the programmed delay depend highly on the D/A converter setting time.

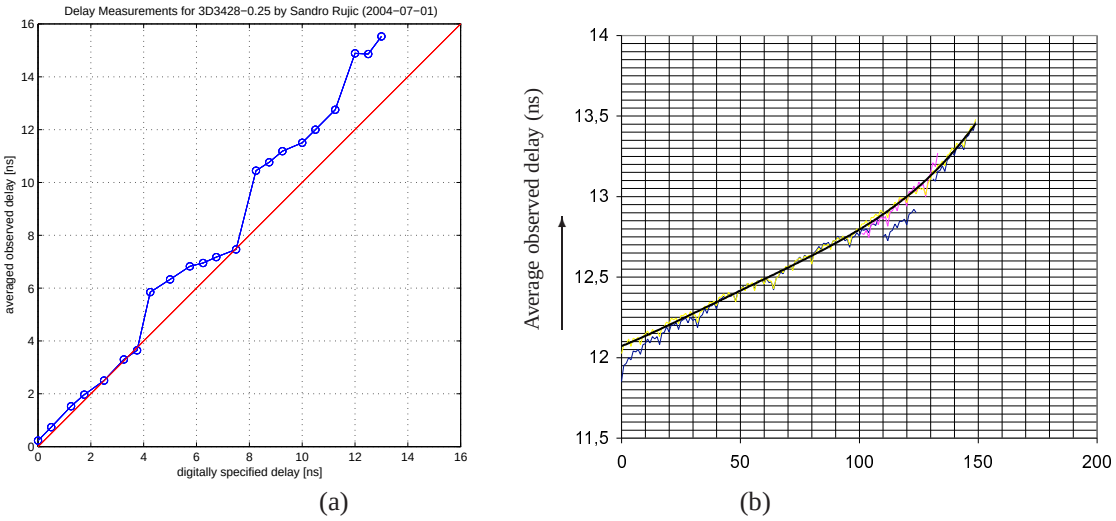

Figure 4: (a) Delay measurement (ns) of 3D2428-0.25, (b) Delay measurement (ns) of Finedelay vs. 8 bit digital input to DAC

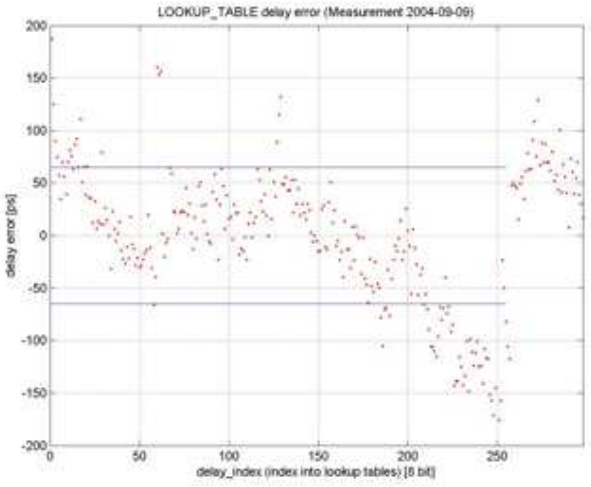

Figure 5: Error of the realised delay shifter (ps)

Acknowledgments

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