ADAPTIVE FILTERS IMPLEMENTATION PERFORMANCES UNDER POWER DISSIPATION CONSTRAINT

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ABSTRACT

Power consumption is an essential criteria in embedded systems. Therefore, it is important to decrease it at every stage of the design flow. It is well known that the choice of a signal processing algorithm has a great impact on the power dissipation. For this purpose, a HLS (High Level Synthesis) CAD (Computer Aided Design) tool (*gaut_ w*) has been developed. It allows to estimate the power dissipation of a dedicated VLSI circuit from the algorithmic description of the application. It also reduces the power dissipation during the architectural synthesis in order to target low power time constrained VLSI circuits. This tool has been applied to different adaptive filters as the *NLMS*, the *BLMS* and the *GAL* filters for a radio-communication application. The power dissipation on a low-power *TMS320C50* DSP (Digital Signal Processing) has been also estimated.

1 INTRODUCTION

Most VLSI researches have been focused on optimising circuit speed and area to perform complex signal processing. Indeed, the rapid advance in VLSI technology and the increase the opertaion number required for recent real time DSP applications imply large chips density and high clock frequency. Then, the minimisation of power dissipation in modern circuits, such as mobile systems, becomes a very important problem and a need of low power CAD tool has emerged.

Section 2 presents our HLS tool into two parts : *Power dissipation estimation* from the behavioural specification and *Power dissipation optimisation* (voltage scaling and selection of operators from a library). Results on adaptive filters will be shown in section 3 before a conclusion.

2 *GAUT_ W* HLS TOOL

Estimating the probable VLSI circuit power dissipation and guiding the design from a behavioural specification of signal and image processing applications represent the two main aims of the *gaut_ w* HLS tool. The behavioural description contains no architectural guidelines. *Gaut_ w* HLS tool can be connected to other softwares such as *Ptolemy* to simulate the behavioural specification or *Compass* to synthesise the circuit from the structural description (Figure 1).

2.1 *Gaut_ w* Overview

Three main parts compose *gaut_ w* :

1. The *power dissipation estimation* [5] gives a fast result from the application behavioural description. This module is composed of an *activity probabilistic estimation* [6] of probable resources in the circuit and a *library* containing all resources caracteristics (average power dissipation, latency time, area).

2. the *power dissipation optimisation* uses the voltage scaling approach which determines the best supply voltage, the selection of the best operators set [2], and manages low power *scheduling* and *assignment* [3] modules

3. the *Gaut architectural synthesis* gives a RTL (Register Transfer Level) description of the circuit that can be synthesised by a logic synthesis tool (*Compass*) [7].

2.2 Power Dissipation Estimation

There are three major sources of power dissipation in digital CMOS circuits due to the gates switching, the direct-path short circuit current and the leakage current. However for CMOS circuits, it is assumed that both short-circuit and leakage power dissipation is negligible. Therefore, the power dissipation is given by (1) [8] :

$$P = C.p.V_{dd}^2.f = C_{eff}.V_{dd}^2.f \qquad (1)$$

where C is the circuit physical capacitance, p the probability of a power consuming transition ($0 \rightsquigarrow 1$), C_{eff} the effective capacitance switched to perform a computation, V_{dd} the supply voltage and f the sampling frequency.

Therefore, the power dissipation is p gates activity dependant. To estimate the average power dissipation

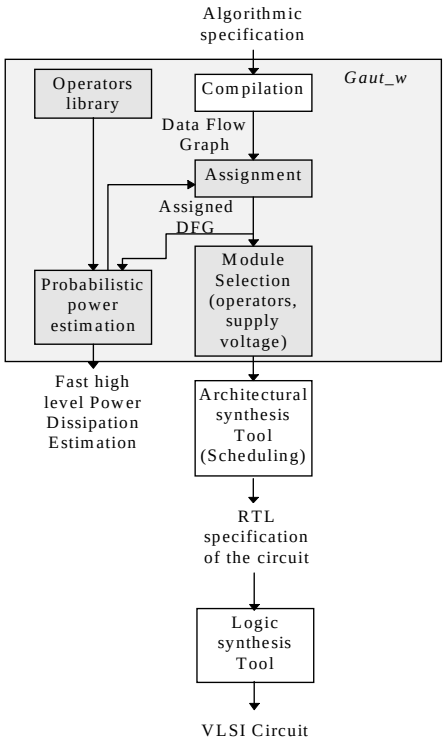

Figure 1: Overview of *Gaut_ w* HLS tool

of resources in the library, each of them has been simulated by the logic simulator *Compass* [5]. The power estimation is the mean result of 5 simulations with 10.000 values length and a 95% confidence interval within 1% tolerated error. This method leads to a good trade-off between the simulation time and the results precision. The library has been done on a $0.8\mu m$ technology. Table 1 shows the library part where T represents the operator latency time, S the gates number and P the power dissipation estimation at 5.5 Volts and with a $1MHz$ sampling frequency.

To estimate the power dissipation at a high level of abstraction, a probabilistic estimation of each resources activity (registers, memory, operators) [5, 6] is needed. Then the probable activity of each probable resource with its average power dissipation allows to estimate the power dissipation of the circuit.

2.3 Power Dissipation Optimisation

Low power optimisation is achieved by reducing either C with technology considerations or C_{eff} during the architectural synthesis.

Voltage scaling has a great impact on the power dissipation because of the quadratic dependence of V_{dd} (1). Unfortunately, reducing V_{dd} increases the T operators latency significantly as when the supply voltage approaches the device threshold voltage V_t (2) [8] :

16 bits operators	T (ns)	S $(10^{-3}mm^2)$	P (μW)
Adder Datapath	14	73	412
Fast Adder Datapath	8.6	122	711
VHDL Adder	18.9	53	229
VHDL Fast Adder	9.9	117	626
Multiplier Datapath	32.3	1337	18827
Pipeline Multiplier Datapath	22	1337	18821
VHDL Multiplier	53.3	1023	11820
VHDL Fast multiplier	33.2	1270	16231
Register	4	70	71
Clock per register	-	-	65
Memory 28*16 bits Static : $36mW$	20	1163	961

Table 1: Operators library part for 0.8 μm

$$T \propto \frac{V_{dd}}{(V_{dd} - V_t)^2} \qquad (2)$$

The power dissipation is minimized through the choice of the best selection of operators in the library and the optimal supply voltage [2]. The method targets time constrained DSP applications. Nevertheless, when V_{dd} decreases, the P power dissipation decreases (1), but the T latency time (2) then the circuit area increase. Therefore, the method allows to attend a good trade-off between power dissipation and area.

Moreover we have developed a simplified operator power dissipation model [3] taking into account the fact that one more entries change between two consecutive operations (when a entry is stable, the power dissipation is minimum). This model has been used to develop low power *scheduling* and *assignment* [3] modules in order to make consecutive operations with a stable entry as often as possible.

3 RESULTS ON ADAPTIVE FILTERS

3.1 Adaptive filters

For a given radio-communication application, different adaptive filters have been specified in this article. The constraints are a 16 KHz sampling frequency and a 64 milliseconds long echo. To cancel this echo, $\frac{1}{(16*10^3)*(64*10^{-3})} = 1024$ points algorithms proposed in the literature have to be used [4]. To compare them according to the power dissipation, two different steps have been carried out :

1. Implantation of 1024 points *NLMS*, *BLMS* and *GAL* algorithms used for a wide band acoustic echo chancellor with the HLS *gaut* and *gaut_ w* tool (with

Figure 2: VLSI circuit for the *NLMS* using *Gaut*

or without power optimisation). Algorithms are specified in behavioural VHDL (about 30-50 lines). The HLS tool generates the VHDL specification of the circuit (about 20000 lines) and the area and the power dissipation estimation. This requires about 30 minutes CPU time. Then, using *Compass* for example, it is possible to obtain the circuit layout (Figure 2).

2. Estimation of the power dissipation of these different algorithms on a low power *TMS320C50* DSP using a 3 Volts supply voltage.

3.2 Power Dissipation Estimation on band filters VLSI wide implementation

The power dissipation using no Area/Time/Power exploration (*Method*1) [7] has been computed in order to compare results in regard with operations numbers and area. Results are presented in Table 3.2. *Power_1* and *Power_2* represent the relative power dissipation without and with power optimisation modules, *Area_1* and *Area_2* the associated VLSI circuit area and *Op_number* the operation number. They permit to calculate the relative power dissipation, area and operation number according to the *NLMS (128 points) algorithm* (Figure 3).

Results shows that the operation number is not accurate enough to compare these four algorithms ; the power dissipation and the area that it is necessary to use a HLS tool to obtain an accurate comparison. For example, when the 1028 points *NLMS* algorithm is used instead of the 128 one, approximately 8 more operations have to be processed, but the power dissipation only increase from a factor 5.5 and the area from a factor smaller than 2. This is due to the fact that the area is the operations numberand time constraint dependant : the multiplier for the 128 points algorithm is only used

	Power (mW) ($Method1$)	Area (mm^2)	Operations number
NLMS (128 points)	126.0	1829	518
NLMS	653.5	3441	4102
BLMS	767.5 ($16KHz$)	4598 ($16KHz$)	16388 ($4KHz$)
GAL	1650.3	7023	6391

Table 2: Results without power optimisation

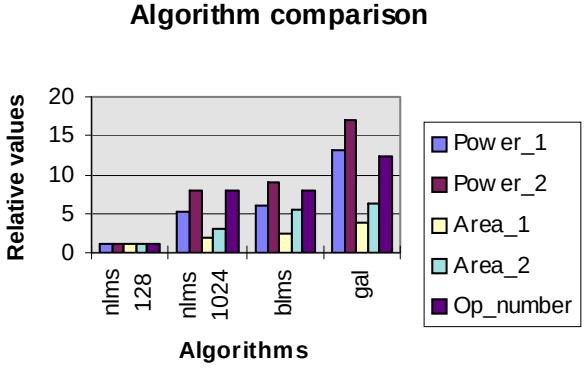

Figure 3: Overview of Results on *NMLS* filters

at 25% while both of them are used at 100% for the 1024 points one. Moreover power dissipation depends on the registers number (*clock tree power dissipqtion*), memory access number and static memory power dissipation [3], and these terms are not linear regarding to the operation number. Another example, *NLMS* and *GAL* algorithms have got a respective complexity of 1 and 1.5, but their relative power dissipation dissipation are 1 and 2.5.

After that, we have used the Area/Time/Power exploration (*Method*2) [2] in order to the power dissipation. Results are presented in Table 2 and the relative values in Figure 3.

Table 2 shows that optimising factor concerning area and power dissipation in not linear regarding to the operation number. For example, *Gaut_w* led to decrease the power dissipation from a 2 factor without any area penalty. This was due to the fact that the time constraint was not difficult to get allowing 3.5 Volts to use power efficient multipliers with higher latency time (without increasing the operator number).

3.3 Power estimation on a *TMS320C50* DSP

Results on these algorithms using the power dissipation estimation of a MIPS (Million Instructions Per Second) on this $0.65\mu m$ DSP have been done. This DSP con-

	Power (mW) ($Method2$)	Area (mm^2)	Power on the *TMS320C50* DSP [9] (W)
NLMS 128	62.8	1829	28.6
NLMS 1024	492.8	5655	226.4
BLMS	566.1 ($16KHz$)	9846 ($16KHz$)	226.2 ($4KHz$)
GAL	1059.1	11397	352.8

Table 3: Results using *Gaut_ w* and a DSP

sumes an average of $1.15mA$ at 3 Volts supply voltage to perform a MIPS [9]. Table 3 compares results on the DSP regarding to a VLSI implementation.

The power dissipation of the *TMS320C50* DSP does not take into account the memory, nevertheless results with *Gaut_ w* use this resource which represents about 50% of the total power dissipation. Moreover, if we consider the relative technology ($0.65\mu m$ for the DSP and $0.8\mu m$) the real power dissipation is greater on the DSP. So, in order to decrease the power dissipation, it is better to have its own VLSI circuit compared to a DSP solution.

4 CONCLUSION

The *gaut_ w* HLS tool permits get both a *fast power dissipation estimation* from an algorithm behavioural description as power dissipation optimization. This tool has been used to compare different adaptive filters for radio-communication applications. Results have shown that a simple algorithms comparison a power dissipation comparison.

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