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ORTHOGONAL CORRECTION IMPLEMENTATION FOR TIME INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS: REALTIME APPLICATION

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ABSTRACT

To significantly increase the sampling rate of an ADC, time-interleaved ADC (TIADC) is an efficient solution. Due to the manufacturing process, the main drawback of a TIADC system is that the M ADCs, which compose this end, are not exactly the same. This means that offset, gain and time mismatch errors are introduced. These errors cause distortions in the output sampled signal and introduce unwanted tones and noise, and hence, reduce the spurious free dynamic range (SFDR) as well as the signal to noise ratio (SNR). In this paper, we propose a new orthogonal digital calibration implementation, for timing skew, offset and gain mismatches, based on Code Division Multiple Access (CDMA) technique. Our calibration is online, this means that errors can be estimated while the ADC is running. Since most of the calibration processes are carried out on the digital outputs, very little change is needed on the analog part of the ADC. Simulation and implementation results show respectively the efficiency of our proposed calibration algorithm and our hardware implementation.

1. INTRODUCTION

Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters are critical components in many communication systems. The current trend is to move more and more of the functionality of a communication system into the digital domain in order to provide an increased flexibility and reduce cost.

In order to comply with modern telecommunication standards and UWB applications, a high-speed and high-resolution analog-to-digital conversion is needed. One way to increase the sample rate beyond its production limits is to exploit parallelism, e.g., in a time-interleaved manner [1]-[3]. For this purpose several channel analog-to-digital converters (ADCs) are operated in parallel with the same sampling rate but with phase shifts to build a time-interleaved ADC. As a result, the sample rate is increased by the number of channels.

These investigations are issued from the originally work of Black and Hodges [4] about TIADC (Fig. 1). The TIADC system works as follows:

- the input signal is connected to all the ADCs,
- if the TIADC is composed of M ADCs, each of them works with a sampling interval of MT_s, where $T_s = 1/F_s$ is the sampling rate of the overall system,
- the clock signal of the kth ADC is delayed with kT_s.

Ideally, the ADCs should have the same characteristics, and should sample the input signal with timing phases uniformly spaced in time.

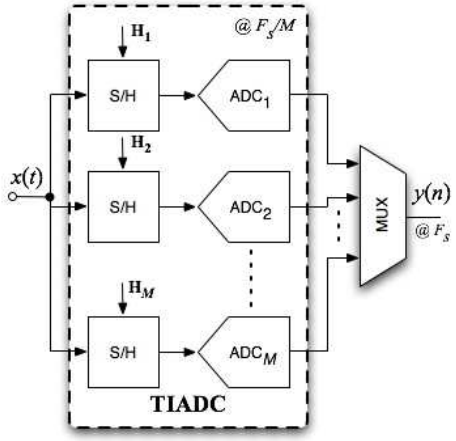

Figure 1 - Time-interleaved ADC architecture

Unfortunately, the channel ADCs are not identical and due to fabrication imperfections additional mismatch effects decrease the performance. The three main mismatch errors,

- *Offset errors;*
- *Gain errors;*
- *Timing errors (clock skew* and *random jitter*).

detailed in [5], will be treated in this paper.

The resulting gain, offset and timing mismatches can degrade performance significantly [5], so they need to be estimated and corrected.

With a sinusoidal input, the mismatch errors can be seen in the output spectrum as distortion. With input signal frequency f_0, the gain and time errors cause distortion at the frequencies $kF_s/M \pm f_0$, whereas offset errors cause distortion at kF_s/M, where $k = 1, 2, \cdots, M$. Fig. 2 shows a TIADC output spectrum composed of 4 ADCs.

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In this paper, a digital calibration implementation method for TIADC based on orthogonal code properties is introduced. Some works have already been done on this subject [6] but with only offset and gain error calibrations. Using the same approach, we have developed [7] a new algorithm allowing a total online digital calibration (time, offset and gain).

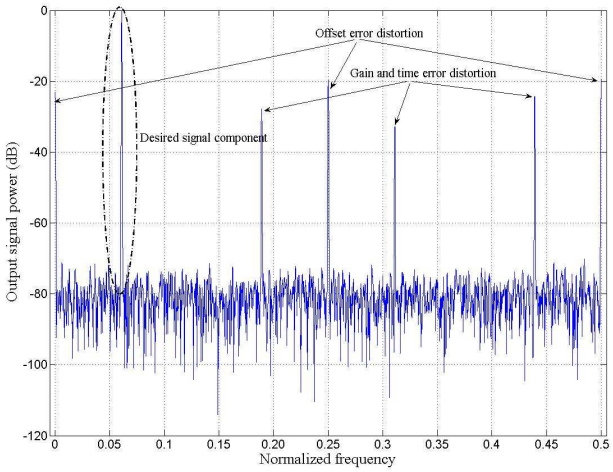

Figure 2 - Output spectrum from TIADC system composed of 4 ADCs.

The utility of orthogonal sequences in data-channel separation has been proved, as the case of spread-spectrum like CDMA [8] used for example in wireless and optical communications. In this paper, we propose to use separation property of orthogonal sequences in order to uncorrelate the contributions of time skew, offset and gain mismatches.
The paper is organised as follows. In section II, description and simulation result performances of our orthogonal online digital calibration algorithm is described. The proposed hardware implementation design and results will be showed in section III and finally section IV presents the conclusion.

2. ORTHOGONAL CALIBRATION: ALGORITHM DESCRIPTION AND PERFORMANCES

The TIADC input signal will be noted,

$$x(t) = A \times \sin(2\pi f_0 t) \tag{1}$$

where A and f_0 are respectively the input signal maximal amplitude and frequency. *M* denotes the number of ADC in the TIADC, and the nominal sampling period of the overall system is T_s. ADC resolution will be noted n_b and time vector acquisition length (FFT size) *L*.

G_k, O_k and Δt_k represent respectively, gain, offset and clock skew associated to the *k*th ADC, with $1 \le k \le M$.

G_k and O_k are range between ± 5 LSB.

Random jitter δt_k is assumed to have a uniform distribution within a range of $\pm 0.5\%$ of the sampling period, i.e. $\delta t_k \in \left[-0.005T_s, +0.005T_s\right]$. Clock skews are supposed to be within the same range with different fixed value for each ADC.
We assume throughout this paper that $x(t)$ is bandlimited to the Nyquist frequency of the TIADC. We suppose that the errors (timing skew, offset and gain) are static or slowly time varying. It means that these errors can be assumed to be constant for the same ADC from one cycle to the next over an interval of some million samples.

2.1 Algorithm description

In this section, we propose a new online calibration method. The algorithm is based on orthogonal properties between two vectors, ***B*** and ***C*** of length *L*, defined such as:

$$\sum_{n=0}^{L-1} B(n)C(n) = 0 \tag{2}$$

and

$$\sum_{n=0}^{L-1} B(n)B(n) = L \quad \text{and} \quad \sum_{n=0}^{L-1} C(n)C(n) = L \tag{3}$$

with $B(n) = (-1)^n$ and $C(n) = 1,\ \forall\ 0 \le n \le L-1$.

Just before analog to digital conversion, the input signal of length *L* is multiplied by ***B***, on each TIADC channels. So, the *n*th input sampling signal from the *k*th ADC is:

$$x_{k,\tilde{n}}(n) = A \times B(n) \times \sin(2\pi f_0 \tilde{n} T_s) \tag{4}$$

with $\tilde{n} = (k + Mn)$, and $0 \le n \le L-1$

In practice, it is important to note that ***B*** will be an analog square signal of period MT_s, range between $\pm FS/2$ where *FS* is the ADC full-scale range.

If $y_k(n)$ denotes the *n*th output sampling signal from the *k*th ADC, we can write:

$$y_k(n) = \tilde{x}_{k,\tilde{n}}(n)B(n) + O_k \tag{5}$$

where,

$$\tilde{x}_{k,\tilde{n}}(n) = AG_k \sin(2\pi f_0(\tilde{n}T_s + \Delta t_k + \delta t_k)) \tag{6}$$

By using sin(*a*+*b*) trigonometry property, we can rewrite (6) as:

$$\tilde{x}_{k,\tilde{n}}(n) = AG_k \begin{pmatrix} \sin(2\pi f_0 \tilde{n} T_s)\cos(2\pi f_0(\Delta t_k + \delta t_k)) \\ +\cos(2\pi f_0 \tilde{n} T_s)\sin(2\pi f_0(\Delta t_k + \delta t_k)) \end{pmatrix} \tag{7}$$

As $2\pi f_0(\Delta t_k + \delta t_k) \ll 1$, using the first term of sine and cosines Taylor developments, (5) becomes:

$$\begin{aligned} y_k(n) \simeq\ & AG_k B(n)\sin(2\pi f_0 \tilde{n} T_s) \\ & + 2\pi f_0 AG_k B(n)(\Delta t_k + \delta t_k)\cos(2\pi f_0 \tilde{n} T_s) \\ & + O_k \end{aligned} \tag{8}$$

2.1.1 Offset estimation

Generally, calibration process needs error estimation phase before correction. The first step of the algorithm proposed is to estimate the offset, which is easily done by the following relation:

$$\hat{O}_k = \frac{1}{L}\boldsymbol{y}_k \times \boldsymbol{C}^T \tag{9}$$

2.1.2 Gain and clock skew estimation

The second step is dedicated to gain and clock skew estimation, which implies offset cancellation. This is done using the zero mean property of $\boldsymbol{B}$:

$$\tilde{\boldsymbol{y}}_k = \frac{1}{L}\boldsymbol{y}_k \boldsymbol{B}^T \tag{10}$$

With relation (8), we can write the nth sample of (10) as:

$$\begin{aligned}\tilde{y}_k(n) &= AG_k \sin(2\pi f_0 \tilde{n} T_s) \\ &+ 2\pi f_0 A G_k (\Delta t_k + \delta t_k)\cos(2\pi f_0 \tilde{n} T_s)\end{aligned} \tag{11}$$

The previous equation shows the correlation between $(\Delta t_k + \delta t_k)$ and G_k leading to a linear equation system with two unknowns: $(\Delta t_k + \delta t_k)$ and G_k. This problem will be solved using matrix notations. Let us consider the following vectors:

$$\begin{cases}\boldsymbol{V}_k = \left[V_{k,k}(0), \cdots, V_{k,\tilde{n}}(n), \cdots, V_{k,k+M(L-1)}(L-1)\right] \\ \boldsymbol{W}_k = \left[W_{k,k}(0), \cdots, W_{k,\tilde{n}}(n), \cdots, W_{k,k+M(L-1)}(L-1)\right]\end{cases} \tag{12}$$

where

$$V_{k,\tilde{n}}(n) = A\sin(2\pi f_0 \tilde{n} T_s)$$

$$W_{k,\tilde{n}}(n) = A\cos(2\pi f_0 \tilde{n} T_s)$$

(11) becomes:

$$\tilde{\boldsymbol{y}}_k = G_k \boldsymbol{V}_k + G_k \overbrace{2\pi f_0 (\Delta t_k + \delta t_k)}^{T_k} \boldsymbol{W}_k \tag{13}$$

As (13) is over determined, two auxiliary equations (14) and (15) were formed:

for $0 \le n \le L/2 - 1$,

$$\tilde{\boldsymbol{y}}_k^{(1)} = G_k \boldsymbol{V}_k^{(1)} + G_k T_k \boldsymbol{W}_k^{(1)} \tag{14}$$

and for $L/2 \le n \le L - 1$,

$$\tilde{\boldsymbol{y}}_k^{(2)} = G_k \boldsymbol{V}_k^{(2)} + G_k T_k \boldsymbol{W}_k^{(2)} \tag{15}$$

with $\tilde{\boldsymbol{y}}_k = \left[\tilde{\boldsymbol{y}}_k^{(1)}\ \tilde{\boldsymbol{y}}_k^{(2)}\right]$, $\boldsymbol{V}_k = \left[\boldsymbol{V}_k^{(1)}\ \boldsymbol{V}_k^{(2)}\right]$ and $\boldsymbol{W}_k = \left[\boldsymbol{W}_k^{(1)}\ \boldsymbol{W}_k^{(2)}\right]$.

Finally, by combining (14) and (15), it has been shown that analytical estimations of clock skew and gain are:

$$T_k = \frac{m_{\tilde{y}_k^{(2)}} m_{\boldsymbol{V}_k^{(2)}} - m_{\tilde{y}_k^{(1)}} m_{\boldsymbol{V}_k^{(2)}}}{m_{\tilde{y}_k^{(1)}} m_{\boldsymbol{W}_k^{(2)}} - m_{\tilde{y}_k^{(2)}} m_{\boldsymbol{W}_k^{(1)}}},\ G_k = \frac{m_{\tilde{y}_k^{(1)}}}{m_{\boldsymbol{V}_k^{(1)}} - T_k m_{\boldsymbol{W}_k^{(1)}}} \tag{16}$$

where $m_u = \frac{2}{L}\sum_{n=0}^{L/2-1} u(n)$.

2.1.3 Calibration process

Finally we obtain the corrected output digital signal:

$$\hat{\boldsymbol{y}}_k = \left(\boldsymbol{y}_k - \hat{O}_k \boldsymbol{C} - T_k \boldsymbol{W}_k\right)/G_k \tag{17}$$

Calibration process leads to cancel offset, gain and clock skew mismatch errors. We can remark that relation (11) proposes a direct cancellation of the offset. So, for the architecture implementation, a simplification of (17) could be done using (11) instead of (8). Thus (17) becomes:

$$\hat{\boldsymbol{y}}_k = \left(\tilde{\boldsymbol{y}}_k - T_k \boldsymbol{W}_k\right)/G_k \tag{18}$$

2.2 Algorithm performances and Simulation results

To evaluate the efficiency of the algorithm presented in this paper, a time-interleaved ADC system composed by two ADCs has been simulated. We proposed to show only the simulation results about clock skew estimation. More simulation results are proposed in [7].

In these conditions, fig. 3 shows sampling and input frequency ratio influence on the estimation.

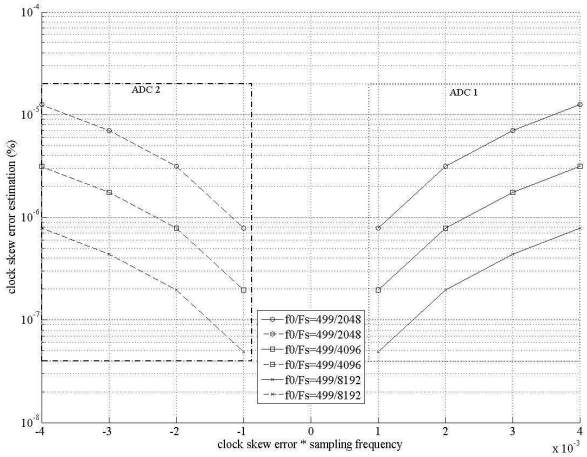

Figure 3 - Phase errors estimation, sampling frequency impact. TIADC with M=2, 2048 FFT points, n_b=8 bits

Error estimation was computed by:

$$\left|\frac{\text{theoretical value} - \text{estimated value}}{\text{theoretical value}}\right| (\%)$$

and clock skew was set to:

$\Delta t_1 = -\Delta t_2 = \left[0.1,\ 0.2,\ 0.3, 0.4\right] T_s / 100$.

The results (Fig. 4 (a), (b)) show that SFDR improves 38.25dB and SNR 1.5dB. Also, we can see that distortions are completely cancelled.

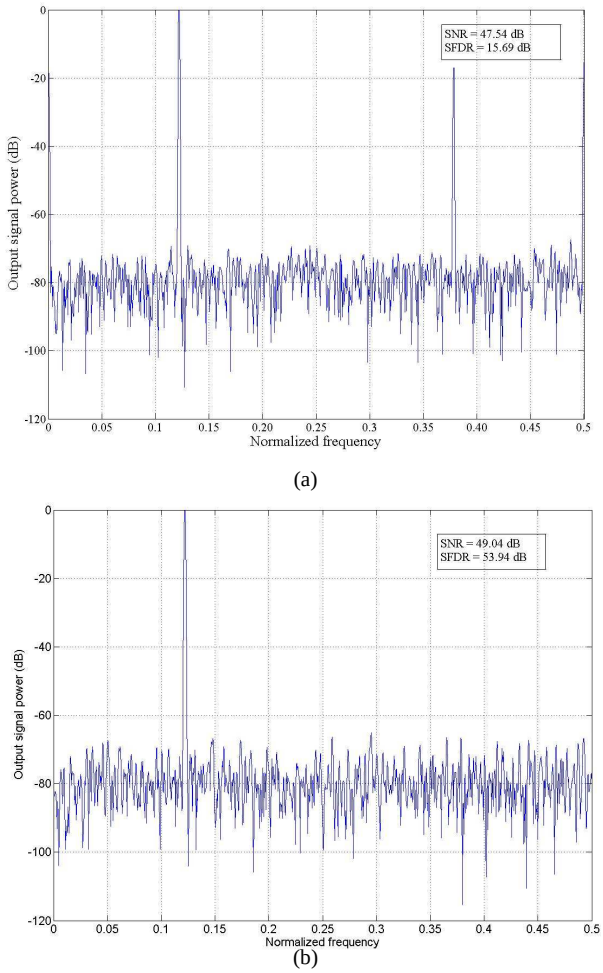

Figure 4 - FFT spectrum before (a) and after (b) calibration. TIADC with M=2, 2048 FFT points, n_b=8 bits, @ -1dB FS

3. IMPLEMENTATION DESIGN AND RESULTS

To evaluate the real-time hardware effectiveness of the proposed signal error correction, several experiments targeting FPGA components were made in order to estimate the possible implementation characteristics. This step is necessary as the proposed approach has been developed to compensate high frequency TIADC systems. These experiments aim to compare different architectures using different fixed point formats.

The target technology is Xilinx Virtex-4 Pro XC2VP100 FPGA. Results were obtained for custom handwritten circuits implemented using fully pipelined hardware operators for maximal frequency performances. The power consumption and the area reduction are not addressed in this work as the main objective is to provide the greater throughput. The architecture logic synthesis was performed using Xilinx ISE 9.2i tool.

The main features of these architectures are summarized in Table 1, together with the synthesis results of our solution mapped onto a Xilinx Virtex5 FPGA device. The Virtex-5 family is the fifth generation in the Virtex series. Built upon 65nm technology, the Virtex-5 family is well known from digital hardware designers as it is optimized for high-speed logic and digital signal processing (DSP), embedded processing.

The implementation schematic of the proposed orthogonal algorithm is presented fig. 5.

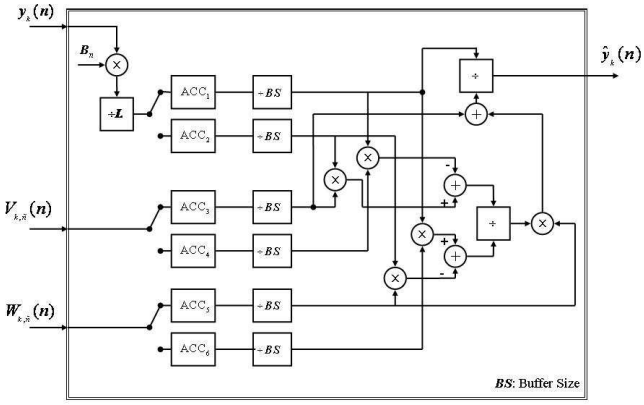

Figure 5 – Implementation design

The hardware operators included in the design have been optimized to reduce as possible their critical path. All the operators (adder, accumulator, multiplier and divider) have been designed in a pipeline fashion to boost the circuit performances.

In the experiments, the architecture was declined in different versions depending of the fixed point bitwidth and depending of the accumulator length (buffer size). These architectures provide interesting compromises between the output value precision (output binary format), the area and the computation latency. The results provided in table 1 proof that the algorithm may be implemented in a common FPGA consuming about 25% of the slices and using high clock frequency.

Table 1 – FPGA synthesis results

		Results				
Buffer size	**Output binary format**	**Latency (clock cycle)**	**throughput (Gb/s)**	**Freq. (MHz)**	**Area slice registers**	**Slice LUTs**
32	8.6	116	4,7	333,33	2984	3668
	8.7	119	5	333,33	3086	3812
	8.8	122	5,3	333,33	3188	3956
64	8.6	148	4,7	333,33	2984	3684
	8.7	151	5	333,33	3086	3828
	8.8	154	5,3	333,33	3188	3972
128	8.6	212	4,7	333,33	2984	3716
	8.7	215	5	333,33	3086	3860
	8.8	218	5,3	333,33	3188	4004

The unchanging frequency value shows that our architecture critical path is independent of the output binary format.

The results, fig. 6 and 7, prove that for this particular application, 16-bit fixed point representation is sufficient to achieve the fixed-point representation performances and thus it has been adopted for the processing blocks here described.

Moreover we can see from previous results that we may introduce, for performance raisons, up to 3 computation cores a single FPGA Virtex-5 for parallel orthogonal algorithm computations. In this case a single Virtex 5 FPGA provides a correcting throughput of 3×333.33 Ms/s (1 Gs/s).

The output data from the FPGA are downloaded with a serial link and used to draw fig. 6. In fact, fig. 6 shows the output spectrum directly obtained with the FPGA output samples in 8.6 format. Distortions are cancelled and the SFDR improvement is about 12 dB.

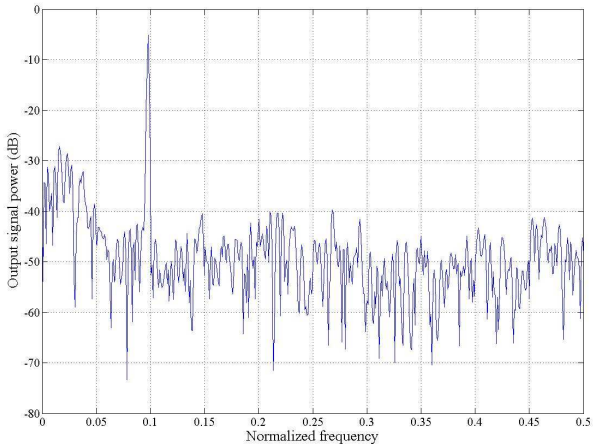

Figure 6 – FFT spectrum after calibration TIADC, *M*=2, 1024 FFT points, n_b=8 bits, @ -5dB FS, 8.6 precision

Fig. 7 shows the output binary format influence on the SNR. We can see that more precise is the output format, better is the SNR. Moreover for an output binary format of 8.8, the SNR improvement, between a buffer size of 32 and 128, is 11dB.

4. CONCLUSION

In this brief, a hardware implementation for a digital calibration technique to compensate mismatch errors in TIADC is presented.

These calibration techniques have a minimal impact on analog complexity and most of calibration and processing steps are carried out in digital domain. Regardless to the proposed hardware implementation, complexity and performances, and to the simulation results, we are able to conclude on the great effectiveness of our technique.

Future work consists:

- to increase the output binary format to analyse the compromise between FPGA synthesis results (area, freq., …) and the (SNR, SFDR) performances,
- to improve the implementation design with a static (magnitude sweep) and a dynamic (frequency sweep) analysis, in order to evaluate our algorithm efficiency in SNR and SFDR.

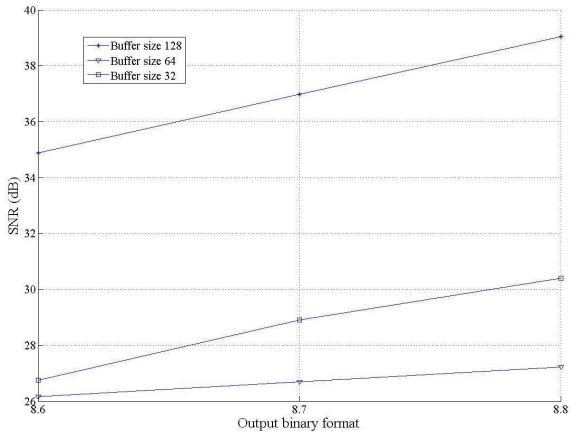

Figure 7 – Output binary format influence on SNR. *M*=2, 1024 FFT points, n_b=8 bits, @ -5dB FS, $f_0/F_s = 0.1$

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