AN APPROACH FOR REAL TIME PROTOTYPING OF MIMO-OFDM SYSTEMS[1]

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ABSTRACT

With multiple-input, multiple-output (MIMO) transmission, impressive capacity or diversity gains can be achieved compared to single antenna systems. We have conceived and implemented a generic platform that enables real-time wireless MIMO transmission. The platform supports the integration and the evaluation of transmit and receive spatial multiplexing and spatial diversity processing techniques for MIMO-OFDM systems in a wireless environment. The platform is based on modular multi-FPGA and multi-board designs with support for high-speed serial connection links between the boards. This paper describes the platform integration of a 2-antenna base station using MIMO transmit processing including special front-end techniques for the exploitation of channel reciprocity in time division duplex (TDD) schemes.

1. INTRODUCTION

MIMO-OFDM is an attractive technique to enhance the capacity of future wireless LANs since space multiplexing increases the spectral efficiency on top of time-frequency and since OFDM modulation mitigates the frequency selective channel fading.

The spatial multiplexing algorithms can be applied in the transmitter (pre-compensation) or in the receiver (post-compensation). The MIMO transmit processing can also be used in the base station (BS) as a space division multiple access (SDMA) technique to enhance the link capacity by serving several single-antenna users at the same time and in the same bandwidth. For both MIMO pre- and post-processing techniques the channel state information is needed. The analytical performances of these spatial multiplexing algorithms are well known. However they are based on models of the indoor channel. Mostly these models do not include the front-end impairments such as phase noise and amplifier non-linearity. Therefore, new challenges are to practically implement the MIMO modem and to quantify the enhanced performance in a real wireless transmission link.

We have developed a real time prototyping platform for high data rate communication systems. The platform is called PICARD [1]: "Platform for Integrated Communication Application, Research and Demonstration".

The example application on the proposed platform is a SDMA system consisting of a 2-antenna BS serving two Hiperlan2 WLAN mobile user terminals (MT). The system operates at 5 GHz in a bandwidth of 20 MHz and supports a maximum downlink data rate of 2 times 54 Mbps. Existing demonstrators are focussing on spatial diversity techniques at the receiver side to enhance the capacity and on space time block codes to exploit spatial diversity [2]. The SDMA demonstrator, that we are building, has the benefit that all the processing power is located in the transmitter of the BS while the user terminal can remain at low complexity, low cost and low power. However, the MIMO transmit processing is more difficult to implement because of the lack of instantaneous channel information at the transmitter. In our implementation, the channel information is retrieved from the uplink and an on-line calibration technique is developed to match the BS transmit and receive antenna branches in amplitude and phase over the entire bandwidth

The performance of the SDMA algorithms is evaluated in real-time on the platform by emulation of a 2-antenna wireless channel. The paper is organized as follows. Section 2 gives an overview of the MIMO algorithms with transmit processing and describes the impact of non-reciprocity on the performance. Section 3 discusses the front-end calibration technique to exploit the channel reciprocity. Section 4 describes the prototyping platform and the hardware chosen to construct it. Section 5 outlines the integration of a 2-antenna BS using MIMO transmit processing with front-end calibration. An overview is given of the required hardware resources for field programmable gate arrays (FPGA). Finally, conclusions are given in section 6.

2. OVERVIEW OF MIMO ALGORITHMS WITH TRANSMITTER PROCESSING

The system model is described as an OFDM/SDMA system with A antennas at the base station and U single antenna terminals. The model applies equally well to a MIMO transmit processing set-up with A transmit antennas and U receive antennas.

[1] This work was partly funded by IWT/Medea+ UNILAN A105 project

In the downlink a per sub-carrier spatial pre-filter is applied on the transmitted symbols in order to separate the signals for the U user terminals. We consider a class of pre-filters that are linear, meaning that pre-filtering is achieved by a multiplication of the transmit symbol vector by a matrix, as follows:

$$\mathbf{y}^{DL} = \mathbf{H}^{DL} \cdot \mathbf{F} \cdot \mathbf{x}^{DL} + \mathbf{n} \qquad (1)$$

where $\mathbf{x}^{DL}$ is the column vector of the U frequency domain streams at sub-carrier n transmitted by the BS, $\mathbf{y}^{DL}$ is the column vector on the A antenna branches of the BS. For the calculation of the pre-filter matrix F, it is assumed that the downlink channel is the transpose of the uplink channel. In (1) the dependency on the sub-carrier index is dropped for clarity.

In [3] the performance of the zero-forcing and MMSE Wiener pre-filters are evaluated based on Monte-carlo simulations. For full system load and uncoded QAM-64 modulation, the MMSE pre-filter outperforms the zero-forcing filter with a gain of 3dB at 10^{-3} BER for the Hyperlan2 class A channel parameters. The zero-forcing pre-filter attempts to perfectly diagonalize the channel matrix and is given by:

$$\mathbf{F}_{ZF} = \left(\mathbf{H}^{DL}\right)^{-1} / \left\| \left(\mathbf{H}^{DL}\right)^{-1} \right\|_{F} \qquad (2)$$

The pre-filter is normalized with the Frobenius norm of the inverse of the channel matrix such that the total transmit power is constant. Hence, the quality of the link decreases when the channel matrix is nearly singular. A better solution than perfect diagonalization consists in using a pre-filter that trades off noise and multi-user interference. This can be optimally achieved by resorting to a Wiener pre-filter, similar to the conventional MMSE post-filter. The MMSE pre-filter is given by:

$$\mathbf{F}_{MMSE} = \mathbf{H}^{DL^H} \left(\mathbf{H}^{DL} \mathbf{H}^{DL^H} + \sigma^2 \mathbf{I}_{UxU} \right)^{-1} \qquad (3)$$

where I_{UxU} is the UxU identity matrix and σ^2 is the variance of the receiver noise. This pre-filter allows a little amount of multi-user interference, equal to the receiver noise. Note that accurate knowledge of σ^2 is not required and a rough estimate is sufficient.

When the transpose of the uplink channel estimation is used to pre-compensate the downlink user interference, the channel is assumed to be reciprocal and static for the time-division duplex scheme. The channel is composed of the propagation channel between the antennas, the antennas themselves and the transceiver RF and analog circuits. Taking the transceiver transfer functions at both sides of the link into account, equation (1) can be refined to (4):

$$\mathbf{y}^{DL} = \underbrace{\mathbf{D}_{RX,MT} \mathbf{H}^{T} \mathbf{D}_{TX,BS}}_{\mathbf{H}^{DL}} \cdot \underbrace{\mathbf{D}_{RX,BS}^{-1} \mathbf{H}^{-T} \mathbf{D}_{TX,MT}^{-1}}_{\mathbf{F}^{DL} = \left(\mathbf{H}^{UL}\right)^{-T}} \cdot \underbrace{\mathbf{D}_{P}}_{\text{Power}} \cdot \mathbf{x}^{DL} + \mathbf{n} \qquad (4)$$

The complex diagonal matrices $D_{RX,BS}$, $D_{TX,BS}$, $D_{RX,MT}$ and $D_{TX,MT}$ contain the BS and MT front-end transmitter or front-end receiver frequency responses as indicated by the indices. The matrix **H** contains the propagation channel itself, which is reciprocal. As can be seen from equation (4), solely the transceiver at the BS should be matched to have a reciprocal channel, i.e. $\mathbf{D}_{TX,BS} \cdot (\mathbf{D}_{RX,BS})^{-1}$ must be equal to the identity matrix multiplied by a scalar. Usually, the RF and analog circuits are not reciprocal between the transmit and receive paths. Figure 1 shows the effect on non-reciprocity in phase and amplitude on SDMA downlink for QAM64 modulation and Hiperlan2 class A channel parameters. The considered OFDM/SDMA system is a BS with 3 antenna and 2 to 3 MTs. The rms values of the phase difference are indicated in the legend. The amplitude difference is derived from the phase as projection on the real and imaginary axes. The simulation results show that the quality of the link degrades significantly for small phase differences. The degradation is highest for full system load. This indicates that the non-reciprocity causes extra multi-user interference (MUI). The matching accuracy in the BS between the transmitter RF and analog circuits and the receiver RF and analog circuits must be below 0.04 dB and 0.25 degrees.

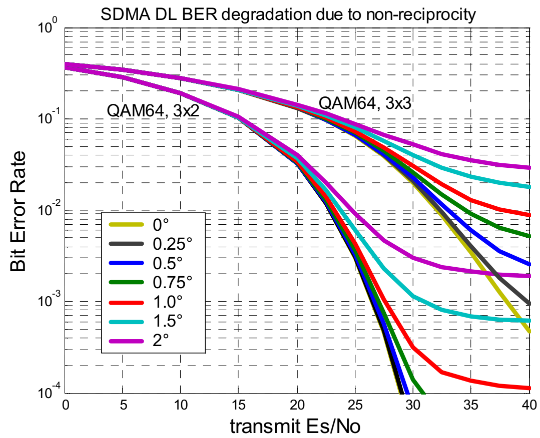

Figure 1 BER Performance Degradation due to non-reciprocity

3. TRANSCEIVER CALIBRATION

The tight overall manufacturing and time variation matching of the RF and analog circuits between the transmitter and receiver are practically not realizable. Therefore, we propose a novel calibration loop that measures the product $\mathbf{D}_{TX,BS} \cdot (\mathbf{D}_{RX,BS})^{-1}$ at the BS so that the mismatches can be pre-compensated digitally at the transmitter. For on-line calibration purposes a reference transceiver is added in the BS. It is connected to the 2 antenna branches with combiner, splitters and cables. The block diagram of the BS with notification of the transfer functions is shown in Figure 2.

The calibration is done in two steps. In the first step a FDMA known signal is generated on a subset of the OFDM carriers in each transmit antenna and received by the reference receiver. This yields the measurement of the following transfer functions:

$$MT1 = T1xC1xRR,\ MT2 = T2xC2xRR \qquad (5)$$

In the second step a known signal is generated in the reference transmitter and received by all receiver antenna branches simultaneously. This yields the measurement of the following transfer functions:

$$MR1 = TRxC1xR1,\ MR2 = TRxC2xR2 \qquad (6)$$

Interpolation over the sub-carriers and averaging over several known symbols is applied to increase the accuracy of the transfer function estimations.
Finally, the following computation is performed:

$$\begin{aligned} \frac{MT1}{MR1} &= \frac{T1xC1xRR}{TRxC1xR1} = \frac{T1}{R1} \cdot \frac{RR}{TR} \\ \frac{MT2}{MR2} &= \frac{T2xC2xRR}{TRxC2xR2} = \frac{T2}{R2} \cdot \frac{RR}{TR} \end{aligned} \qquad (7)$$

In these two expressions, the terms T1/R1 and T2/R2 are the desired results (ratio of transmitter frequency response over receiver frequency response) while the term RR/TR comes from the unknown frequency response of the reference transceiver. However, since both T1/R1 and T2/R2 are multiplied by the same unknown term, this does not introduce MUI. This calibration technique has been implemented on the PICARD platform.
For the hardware implementation of the calibration algorithm special attention has to be paid on the synchronisation offsets and the phase noise offsets between the antenna branches. Synchronisation offsets result in a phase slope across the frequency response in case of timing offset differences or in a phase shift in case of carrier frequency offset differences. It is also required that the transfer function measurements are done simultaneously over all branches so that the impact of phase noise is identical on all branches. When several measurements need to be averaged, phase noise impairments must be carefully dealt with. It is therefore mandatory to use the same local oscillators and clocks in all antenna branches of the BS. In addition, all AGC operating points must be calibrated.

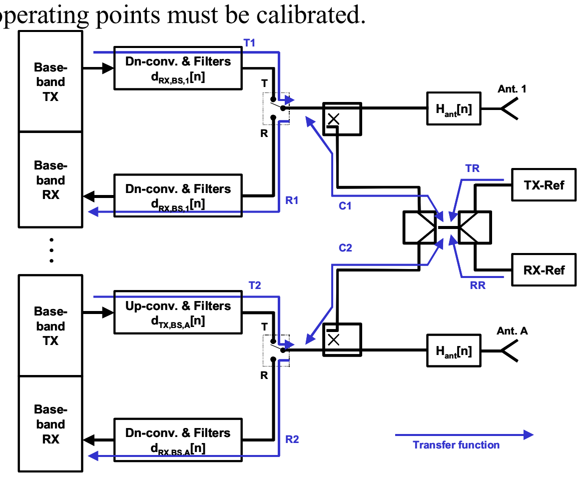

Figure 2 Block Diagram of the Reciprocity Calibration

4. REAL TIME OFDM/MIMO PLATFORM

We have defined platform hardware and software concepts to prototype and demonstrate broadband wireless systems. It is based on modular hardware boards and Linux driver development software. The boards are c-PCI compliant so that they can be plugged in a commercial off-the-shelf rack to build a complete system together with a commercial host c-PCI processor board (Figure 3)

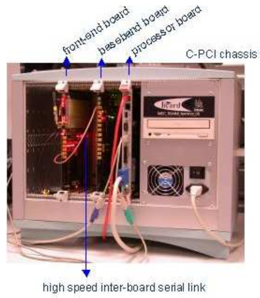

Figure 3 PICARD system prototyping platform

The major challenges in the design an MIMO-OFDM prototyping platform are the availability of hardware resources to implement the complex algorithms and the availability of real time high data rate communication links between components and between boards. Therefore, we have designed two boards following the PICARD modular board concepts (Figure 4). It can be seen that both boards are derived from the same basic schematic netlist. The two boards are general in the sense that both contain configurable hardware (max 2 Xilinx XC2V6000 FPGAs [4]) for the implementation of the digital part of the MIMO modem and that one board has a socket to plug in a daughter board with the antenna array RF front-end.

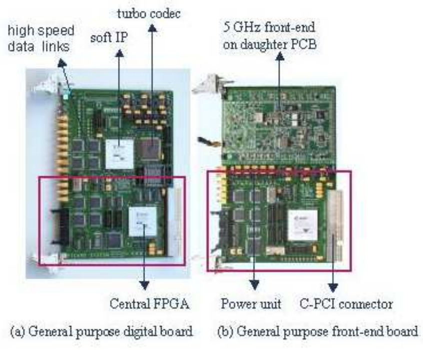

Figure 4 PICARD board library

A complete MIMO system can be prototyped on the platform using one or more boards. The platform concepts foresee dedicated high speed data links (1.4 Gbps per link) between the boards to transfer the payload data without latency. The number of boards depends on the required system processing power and the level of integration of the antenna array. For example the antenna array can be build as a set of single antenna RF boards or can be integrated in one system in package module. We have designed a 5 GHz superheterodyne WLAN transceiver with discrete components. It can be used in a single antenna system or in a multiple antenna system. The platform has the connections to synchronize the ADC and DAC sampling clocks of the antenna branches to a common clock and to steer the phase locked loops of the RF and IF synthesizer with the same reference clock. In this way the antenna branches are synchronized in time and in phase.

On top of the physical MIMO modem layer runs the Medium Access Control (MAC) layer. The non-timing-critical functions such as association and authentication exchanges or data frame preparation run on the host processor. The time critical functions require the MAC to act within microseconds of an event or at precise intervals. For this purpose, we have designed a soft processor core with an optimized architecture and instruction set for fast data shuffling. The MAC soft processor core can be present on each board of the MIMO system. For this, each MAC soft processor core has a timer-counter on which their actions are synchronized.

5. EXAMPLE: 2-ANTENNA MIMO USING TRANSMIT PROCESSING

The high-level functional building blocks of the 2 antenna BS with transmit processing is shown in Figure 5.

At transmit side two user streams are turbo encoded and are in the "MIMO transmit pre-compensation" unit mapped on symbols, MMSE pre-filtered and converted to time domain by IFFT. In the uplink the users are assigned to separate time slots. The incoming user data streams on the 2 antennas are put within the dynamic range of the A/D converter by the automatic gain controllers (AGC). In the TDMA receiver the timing and carrier frequency offset is estimated on the preamble of one antenna and the compensation is done on the streams of both antenna. The channel is estimated on the preambles for each user and for each antenna. These channel estimations are used as input to the MMSE pre-filter to calculate the matrix F_{MMSE} (3). The remainder of the burst contains the user payload data and is in the receiver further demodulated, turbo decoded and passed to the MAC layer.

Two general purpose digital boards are used to integrate the turbo codecs, the MIMO baseband transceiver and the soft MAC processor. The MIMO transmit pre-compensation unit is mapped on one XC2V6000. It uses 49% of the slices and 63% of the multipliers at a 20 MHz clock. The TDMA receiver with channel estimator is mapped on one XC2V6000. It uses 48% of the slices and 86% of the multipliers at 20 MHz clock. The channel estimator is improved with an interpolator that takes the overall channel length into account. .

The 2-antenna transceiver is build from two single antenna 5 GHz front-end boards. The compensation techniques for the front-end imperfections are mapped on the FPGA of the same board. For performance evaluation of the system the antennas are bypassed and the channel emulator is mapped on the FPGA. The channel includes a 9-tap FIR filter modelling a 2x2 antenna multi-path channel, an AWGN generator and a carrier frequency offset generator. It takes 48 % of the slices and 77 % of the multipliers at 80 MHz clock.

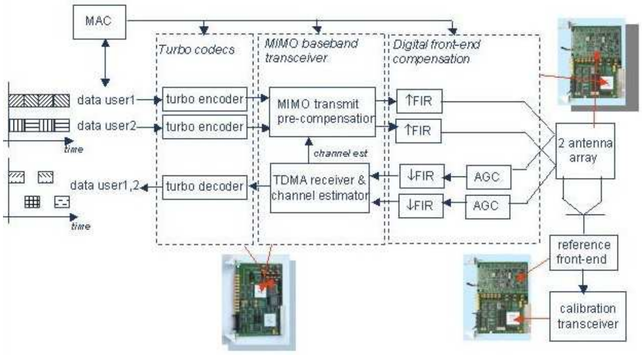

Figure 5 Block diagram of 2-antenna access point

The antenna array is calibrated on-line by means of a 5 GHz reference single antenna front-end board. The calibration transceiver transmits the known calibration signal and calculates the transmitter transfer functions MT1 and MT2. The calibration transceiver function on the reference front-end FPGA takes 53% of the slices and 25 % of the multipliers at 20 MHz clock. The channel estimator in the MIMO baseband transceiver unit is reused during calibration to calculate the receiver transfer functions MR1and MR2. The MAC layer controls the scheduling of the calibration and stores the front-end transfer functions in memory for each AGC setting.

6. CONCLUSIONS

In this paper, we have proposed platform concepts for real time prototyping of MIMO systems. Two boards are designed. One board integrates the radio on a front-end daughter board. The second board integrates the baseband functionality on configurable logic. A 2-antenna MIMO-OFDM system with a doubled downlink capacity compared with IEEE.11a standard is prototyped on the platform. An overview of the hardware resources is given. The system performance is evaluated in real time on an emulated channel model. An on-line calibration algorithm to pre-compensate non-reciprocity between the transmit and receive antenna branches is proposed and is integrated on the platform.

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